

What is claimed is:

- 1 1. A microelectronic die comprising:
 - 2 first and second differential signal lines on a first metal layer of the
 - 3 microelectronic die to carry a differential signal within the microelectronic die, said
 - 4 first and second differential signal lines being substantially parallel to one another;
 - 5 wherein each of said first and second differential signal lines provides a return
 - 6 path for a signal on the other of said first and second differential signal lines, said return
 - 7 path being the predominant return path for each respective signal.
- 1 2. The microelectronic die of claim 1, comprising:
 - 2 at least one trace on a second metal layer of the microelectronic die, said at least
 - 3 one trace being capacitively coupled to and non-parallel with said first and second
 - 4 differential signal lines.
- 1 3. The microelectronic die of claim 2, wherein:
 - 2 said at least one trace is substantially orthogonal to said first and second
 - 3 differential signal lines.
- 1 4. The microelectronic die of claim 2, wherein:
 - 2 said at least one trace includes a data line.
- 1 5. The microelectronic die of claim 2, wherein:
 - 2 said at least one trace includes a power line.
- 1 6. The microelectronic die of claim 2, wherein:
 - 2 said second metal layer is adjacent to said first metal layer.
- 1 7. The microelectronic die of claim 2, wherein:
 - 2 said at least one trace includes multiple traces that are substantially parallel to
 - 3 one another.

1 8. The microelectronic die of claim 2, wherein:
2 said at least one trace provides a return path for a signal on said first differential
3 signal line that has a significantly higher impedance than a return path provided by said
4 second differential signal line.

1 9. The microelectronic die of claim 1, wherein:
2 said first and second differential signal lines are part of a clock distribution
3 network to distribute a clock signal within the microelectronic die.

1 10. The microelectronic die of claim 9, wherein:
2 said clock distribution network uses salphasic clocking techniques to distribute
3 said clock signal.

1 11. The microelectronic die of claim 9, wherein:
2 said clock distribution network includes a clock grid to generate, using said
3 clock signal, a standing wave pattern for use in performing salphasic clocking, said first
4 and second differential signal lines being part of said clock grid.

1 12. The microelectronic die of claim 1, wherein:
2 said first and second differential signal lines provide a point to point signal
3 connection within said microelectronic die.

1 13. A microelectronic die comprising:
2 a clock signal source to provide a clock signal; and
3 a clock signal distribution network to distribute said clock signal to multiple
4 clocked elements within said microelectronic die using salphasic clocking techniques,
5 said clock signal distribution network including at least one on-die interconnect section
6 comprising first and second differential signal lines on a first metal layer of said

7 microelectronic die to carry a differential version of said clock signal, said first and
8 second differential signal lines being substantially parallel to one another.

1 14. The microelectronic die of claim 13, comprising:
2 at least one trace on a second metal layer of said microelectronic die, said at
3 least one trace being capacitively coupled to and non-parallel with said first and second
4 differential signal lines.

1 15. The microelectronic die of claim 14, wherein:
2 said at least one trace is substantially orthogonal to said first and second
3 differential signal lines.

1 16. The microelectronic die of claim 13, wherein:
2 said clock signal is sinusoidal.

1 17. The microelectronic die of claim 13, wherein:
2 said first and second differential signal lines are part of a clock grid within said
3 clock distribution network.

1 18. The microelectronic die of claim 13, wherein:
2 said first and second differential signal lines are part of an H-tree within said
3 clock distribution network.

1 19. A microelectronic die comprising:
2 a differential transmission line having first and second differential signal lines
3 on a first metal layer of the microelectronic die, said first and second differential signal
4 lines being substantially parallel to one another; and
5
6 a differential driver coupled to said differential transmission line to impart a
7 differential signal to said differential transmission line.

1 20. The microelectronic die of claim 19, wherein:
2 each of said first and second differential signal lines provides a return path for
3 a signal on the other of said first and second differential signal lines, said return path
4 being the predominant return path for each respective signal.

1 21. The microelectronic die of claim 19, comprising:
2 at least one trace on a metal layer of said microelectronic die that is adjacent to
3 said first metal layer, said at least one trace being capacitively coupled to and
4 orthogonal to said first and second differential signal lines.

1 22. The microelectronic die of claim 19, comprising:
2 a differential receiver coupled to said differential transmission line to receive
3 said differential signal from said differential transmission line.

1 23. The microelectronic die of claim 19, wherein:
2 said microelectronic die includes microprocessor circuitry.

1 24. The microelectronic die of claim 19, wherein:
2 said differential driver includes a buffer having a small signal differential
3 output.

1 25. The microelectronic die of claim 19, wherein:
2 said differential transmission line is part of an on-die salphasic clock
3 distribution network.